

# CEM11M2



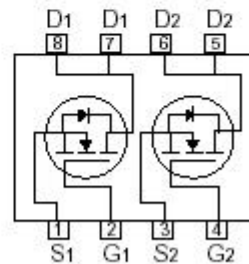
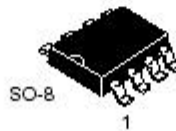
PRELIMINARY

## Dual N-Channel Enhancement Mode Field Effect Transistor

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### FEATURES

- 20V, 6A,  $R_{DS(on)}=25m\Omega$  @ $V_{GS}=4.5V$ ,  
 $R_{DS(on)}=31m\Omega$  @ $V_{GS}=2.5V$ .
- Super high dense cell design for extremely low  $R_{DS(on)}$ .
- High power and current handling capability.
- Surface Mount Package.



### ABSOLUTE MAXIMUM RATINGS ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	20	V
Gate-Source Voltage	$V_{GS}$	$\pm 8$	V
Drain Current-Continuous @ $T_J=125^\circ\text{C}$ -Pulsed <sup>b</sup>	$I_D$	$\pm 6.0$	A
	$I_{DM}$	$\pm 35$	A
Drain-Source Diode Forward Current <sup>a</sup>	$I_S$	1.7	A
Maximum Power Dissipation <sup>a</sup>	$P_D$	2	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient <sup>a</sup>	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$
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## ELECTRICAL CHARACTERISTICS (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ <sup>c</sup>	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	$V_{DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	20			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 20V, V_{GS} = 0V$			1	$\mu A$
Gate-Body Leakage	$I_{GSS}$	$V_{GS} = \pm 8V, V_{DS} = 0V$			$\pm 100$	nA
<b>ON CHARACTERISTICS<sup>b</sup></b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	0.5	0.65	1	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 4.5V, I_D = 6.0A$		20	25	n $\Omega$
		$V_{GS} = 2.5V, I_D = 5.2A$		26	31	n $\Omega$
On-State Drain Current	$I_{D(on)}$	$V_{DS} = 5V, V_{GS} = 4.5V$	20			A
Forward Transconductance	$g_{FS}$	$V_{DS} = 10V, I_D = 6.0A$	7	18		S
<b>DYNAMIC CHARACTERISTICS<sup>c</sup></b>						
Input Capacitance	$C_{ISS}$	$V_{DS} = 8V, V_{GS} = 0V$ $f = 1.0MHz$		1661		pF
Output Capacitance	$C_{OSS}$			470		pF
Reverse Transfer Capacitance	$C_{RSS}$			110		pF
<b>SWITCHING CHARACTERISTICS<sup>c</sup></b>						
Turn-On Delay Time	$t_{D(on)}$	$V_{DS} = 10V,$ $I_D = 1A,$ $V_{GS} = 4.5V,$ $R_{\theta EM} = 6 \Omega$		24	48	ns
Rise Time	$t_r$			20	40	ns
Turn-Off Delay Time	$t_{D(off)}$			76	140	ns
Fall Time	$t_f$			16	32	ns
Total Gate Charge	$Q_g$	$V_{DS} = 10V, I_D = 6A,$ $V_{GS} = 4.5V$		15	20	nC
Gate-Source Charge	$Q_{gs}$			2.6		nC
Gate-Drain Charge	$Q_{gd}$			3.5		nC

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## ELECTRICAL CHARACTERISTICS ( $T_A=25^{\circ}\text{C}$ unless otherwise noted)

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Parameter	Symbol	Condition	Min	Typ <sup>c</sup>	Max	Unit
<b>DRAIN-SOURCE DIODE CHARACTERISTICS<sup>b</sup></b>						
Diode Forward Voltage	$V_{SD}$	$V_{GS} = 0V, I_S = 1.7A$		0.75	1.2	V

### Notes

a. Surface Mounted on FR4 Board,  $t \leq 10\text{sec}$ .

b. Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

c. Guaranteed by design, not subject to production testing.

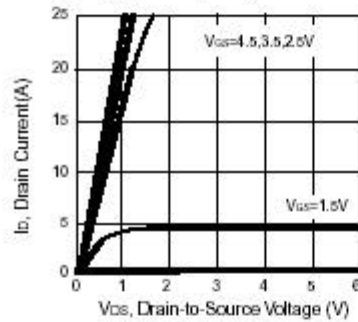


Figure 1. Output Characteristics

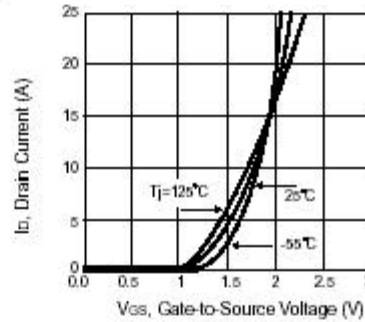


Figure 2. Transfer Characteristics

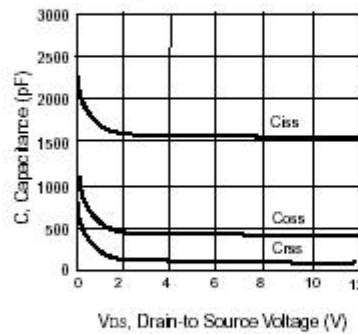


Figure 3. Capacitance

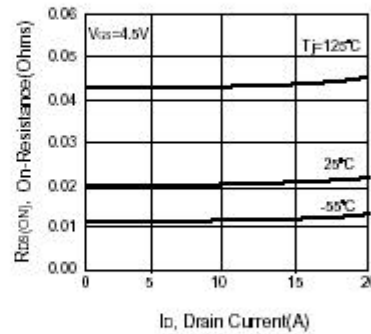
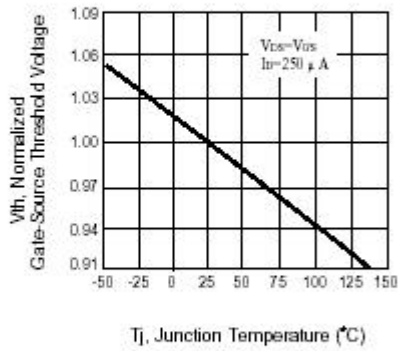
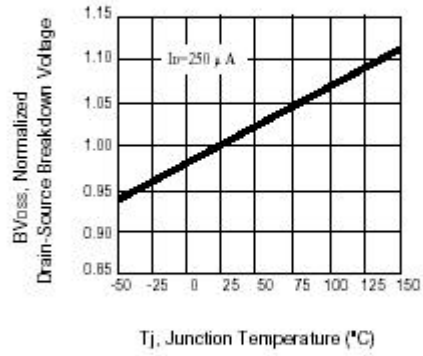


Figure 4. On-Resistance Variation with Drain Current and Temperature

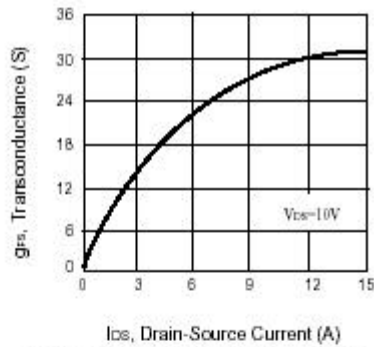
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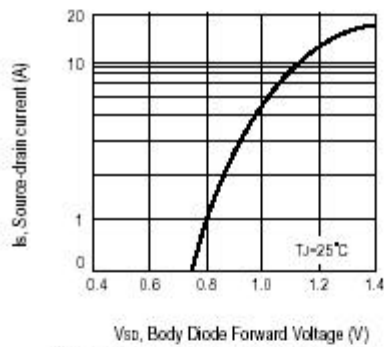
**Figure 5. Gate Threshold Variation with Temperature**



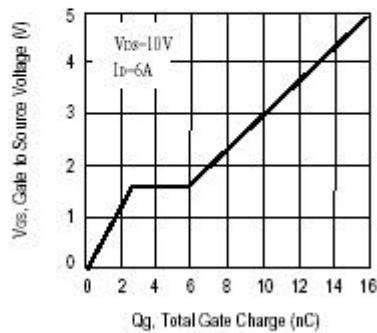
**Figure 6. Breakdown Voltage Variation with Temperature**



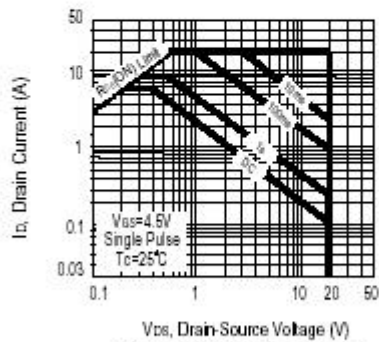
**Figure 7. Transconductance Variation with Drain Current**



**Figure 8. Body Diode Forward Voltage Variation with Source Current**



**Figure 9. Gate Charge**



**Figure 10. Maximum Safe Operating Area**

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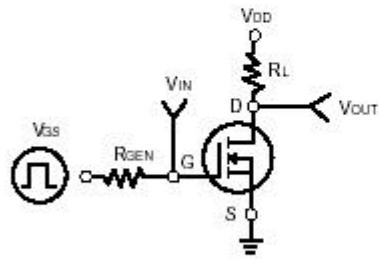


Figure 11. Switching Test Circuit

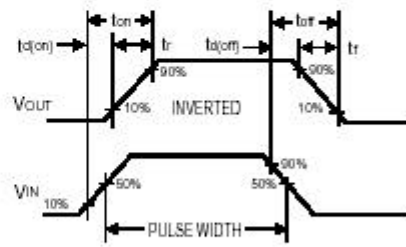


Figure 12. Switching Waveforms

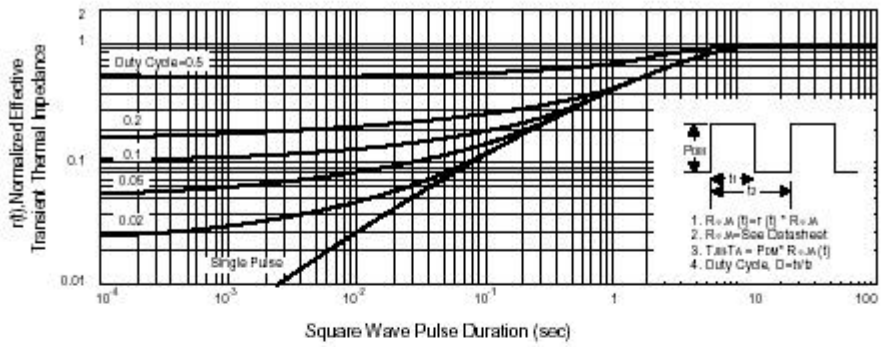


Figure 13. Normalized Thermal Transient Impedance Curve